NEW GaAs PIN DIODES WITH LOWER DISSIPATION LOSS, FASTER SWITCHING SPEED AT LOWER DRIVE POWER

C. BARRATT+, A. CHRISTOU*. N. JANSEN+, R.E. NEIDERT*
M.L. RUESS, JR.*, C.W. YOUNG*

+M/A-COM, Inc.
Burlington, MA 01803

*U.S. Naval Research Lab
Washington, D.C. 20375

ABSTRACT

GaAs PIN diode material with low forward resistance and high Q reverse bias capacitance has been successfully grown for the first time. Static performance data for shunt mounted chips in a microstrip SPST switch show improved insertion loss for the 2-40 GHz range. Dynamic data show switching speed and switch drive power advantages of GaAs over Si for both carrier injection and sweep-out modes of operation.

INTRODUCTION

Gallium arsenide PIN diode wafers with I-layer thicknesses of 8-30 μm have been successfully grown for the first time in a computer controlled GaAs-$AsCl_3$-H_2 vapor phase epitaxial reactor system.* Sequential growth of the N-type, I and P-type on an N-type host substrate is carried out in one single growth process. Silane (SiH_4) and dimethyl-zinc ($(CH_3)_2Zn$) are used as the N and P-type dopant gases, respectively, with carrier concentrations in excess of $10^{18}/cm^3$. The I-layer is intentionally undoped at a carrier concentration of 10^{13} to $10^{14}/cm^3$. The practical upper limit to I-layer thickness grown by this process is 40μm. Both mesa chip PIN and gold plated heatsink (PHS) NIP diodes have been processed and fabricated from these wafers.

The reverse biased breakdown voltage of these devices compares with silicon PIN diodes of equivalent I-layer thickness. Junction capacitances of 0.04 pF to 0.4 pF have been fabricated. The devices typically exhibit forward biased resistance (RF) of 0.8 to 1.5 ohms at I_F of 25mA, and reverse biased resistance (R_R) of 2 ohms at V_R of 0 volts (devices are designed to be punched through at zero bias).

Since GaAs is a direct bandgap semiconductor, injected charge during forward conduction is primarily stored at the NI and IP boundaries with little or no charge stored in the central portion of the I-region, contrary to Si PIN diodes where the maximum stored charge occurs at the center of the I-region. The electron mobility (μ_e) in GaAs is approximately four times that in silicon and the carrier lifetime (τ) shorter; however, the $\mu\tau$ product is about the same as that in silicon. The consequencies are:

1) The higher carrier mobility results in an equivalent reverse biased series resistance (R_R) of approximately half that of silicon.

2) The $\mu\tau$ product results in a forward resistance (R_F) of about 1 ohm, similar to silicon. However, the forward resistance reaches a minimum limiting value at I_F levels typically less than 100mA. Silicon devices will asymptotically approach lower values (few tenths of an ohm) at much higher current drives.

3) For capacitance values fabricated to date, GaAs devices behave more like ideal PIN diodes in that they exhibit no RF dependence on device area.

4) The reverse bias voltage requirements are low (-5V) and the RF reverse switching speed is virtually independent of I-layer thickness, making GaAs PIN's ideal for use with ECL, particularly for thicknesses of 25 μm or less. This same condition holds true for silicon PIN diodes of 6μm maximum thickness and TTL.

RF STATIC PERFORMANCE

Chip diodes have been tested in a shunt mounted low dielectric permittivity (Duroid 5880) microstrip SPST switch circuit. A circuit schematic is shown in Figure 1. The center conductor to ground plane spacing is nominally 0.19 mm. SMA jack to microstrip launchers are employed at the input and output ports. The total microstrip circuit length is 2.5 cm, and is soldered to the bottom of a metal channel 0.13 inch wide to insure only TEM mode propagation at frequencies well above 20 GHz. 40 pF lumped element blocking capacitors are employed on each side of the diode. Diode bias/drive is provided through a 22 turn air core miniature choke with 130 nH inductance at 250 MHz and by-passed to ground through a 390 pF chip capacitor.

RF static performance data for 10 μm PIN and 30 μm NIP diodes over the 2-18 GHz frequency range are plotted in Figures 2 and 3, respectively. The insertion loss of a reference unit which includes all SPST switch elements, but substitutes a 50 ohm section of microstrip line for the diode, are also plotted so that diode contribution to loss can be identified. Isolation data were taken at several current levels and samples are plotted in Figures 2 and 3. While the forward resistance, R_F, of silicon PIN diodes continues to decrease at higher current drives (>200 mA) so that values of 0.5 ohm or less can be achieved, the R_F of GaAs diodes will asymptotically approach some limiting value, typically 0.8-1.0 ohm at current drives of 30-50 mA, depending on the I-layer thickness.

*U.S. Patent, 4,190,470, "Production of Epitaxial Layers by Vapor Deposition Utilizing Dynamically Adjusted Flow Rates and Gas Phase Composition", November 6, 1978.

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By June, 1983, static performance data of 5-10μm GaAs PINs and NIPs will be extended to 40 GHz. The circuit will consist of WR-28 waveguide to low dielectric permittivity microstrip transitions and both SPST and SPDT versions of shunt mounted chips on microstrip.

RF DYNAMIC PERFORMANCE

Switching speed measurements have been performed for all three diodes using the test set illustrated in Figure 4. The figure also defines RF switching speed and total switching speed, which includes a time delay between drive initiation and diode response. The toggle speed for all tests was 1 MHz at a 50 percent duty factor. Test results are plotted in Figures 5 and 6 for the 10μm and 18μm diodes. "Injection" implies forward current flow and "sweep out" reverse bias. The total switching speeds for 10μm GaAs and Si PIN diodes are compared in Figure 5. The reverse bias in all cases was driven to -5 volts and the current varied from 8 to 30 mA. At I_F = 30 mA and V_R = -5V, 10μm GaAs diodes exhibit RF switching speeds of 5 ns and 17 ns for sweep out and injection, respectively. For equivalent Si diodes, the corresponding values are 17 ns and 20 ns. Figure 6 compares 18 μm GaAs NIP performance at V_F = 5V with 20 μm Si PIN diodes at V_R = -5 and -10V. In all cases the GaAs diodes have a faster response time than Si. Note that high power TTL logic is sufficient to drive these devices. The RF switching speeds of all diodes up to 36 μm I-layer are 4-5 ns in the sweep out mode at TTL voltage levels. This is a distinctive advantage over equivalent Si devices.

ACKNOWLEDGEMENTS

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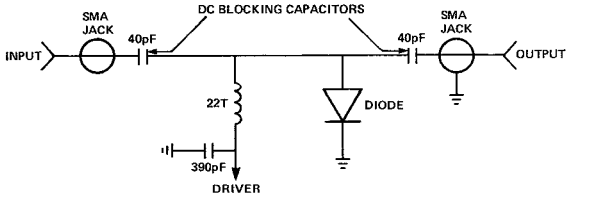


FIGURE 1 SCHEMATIC DIAGRAM OF SHUNT MOUNTED GaAs CHIP PIN/NIP DIODE SPST TEST CIRCUIT

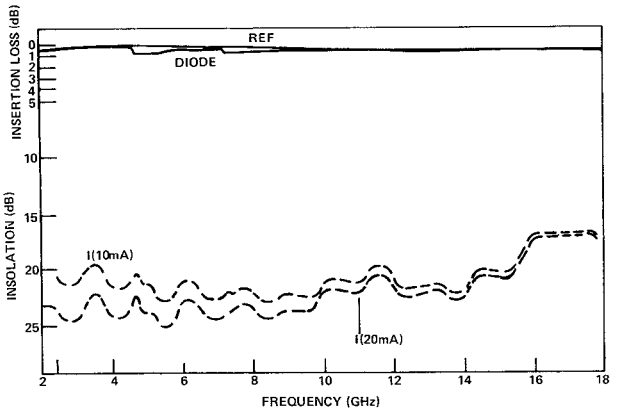


FIGURE 2 PERFORMANCE DATA OF SHUNT MOUNTED 10μm I-LAYER GALLIUM ARSENIDE PIN SPST SWITCH

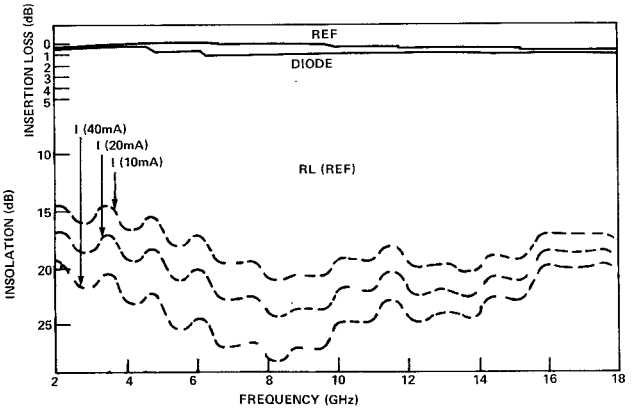
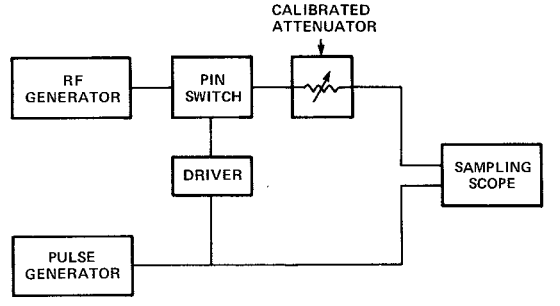


FIGURE 3 PERFORMANCE DATA OF SHUNT MOUNTED 36μm I-LAYER GALLIUM ARSENIDE NIP (PHS) SPST SWITCH.



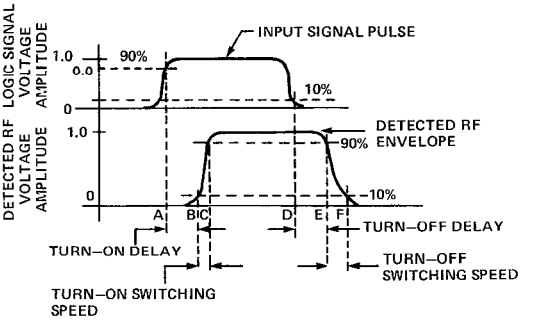


FIGURE 4 SWITCHING SPEED MEASUREMENT AND DEFINITION FOR PIN SWITCH

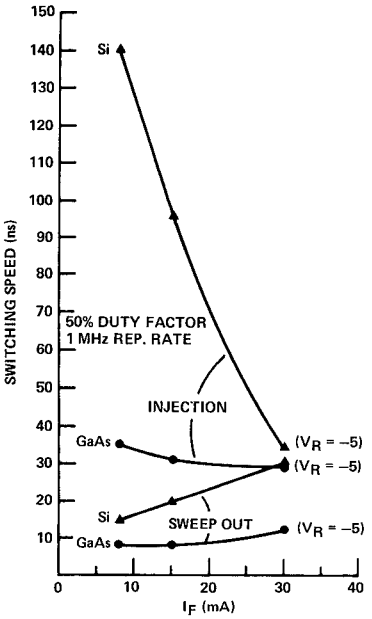


FIGURE 5 TOTAL SWITCHING SPEED RESPONSE OF 10μm GaAs AND Si PIN DIODES

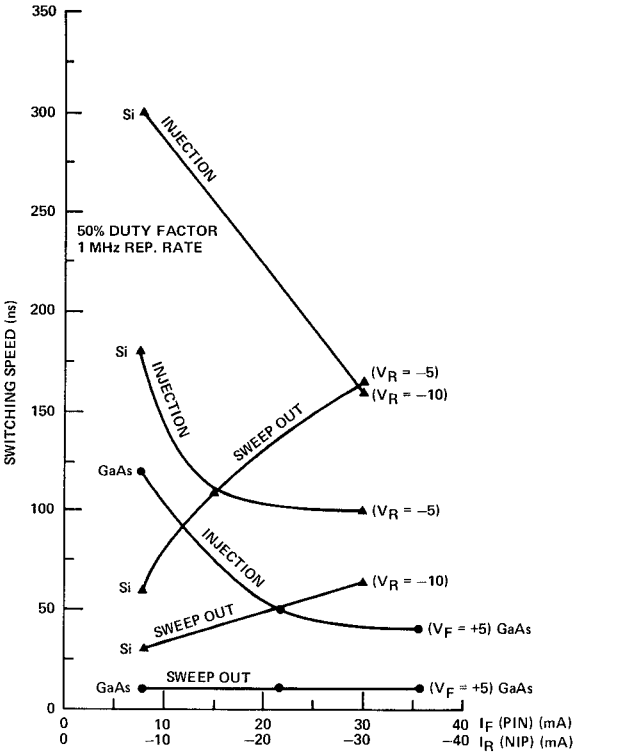


FIGURE 6 TOTAL SWITCHING SPEED OF 18μm GaAs NIP AND 20μm Si PIN DIODES